SAS Israel

S.A.S Advanced Technologies




Company Introduction

www.sas-tech.com

Main Business

Semiconductor **A**dvanced **S**ervices - Post Silicon Engineering

SAS Israel offers a wide range of services under one roof to our customers.

Starting with Engineering sale support, Onsite Field Support Engineers (FSE)

Our partners around the world

- **Leeno industrial inc.(S. Korea) –** For Build to spec Logic , RF, IC Test sockets.
- **Caliber Interconnect Solutions (India) -** For Design and Simulation before production and final test.
- **Hon Prec (Taiwan)–** Hon Prec Handlers

HIGHWIRE

Gold Award Winner

Product Testing

- Full in-house product validation , per customer specification.
- Write test plans, Make sure it covers all the important requirements.

SAS Team members

Leadership and Reporting

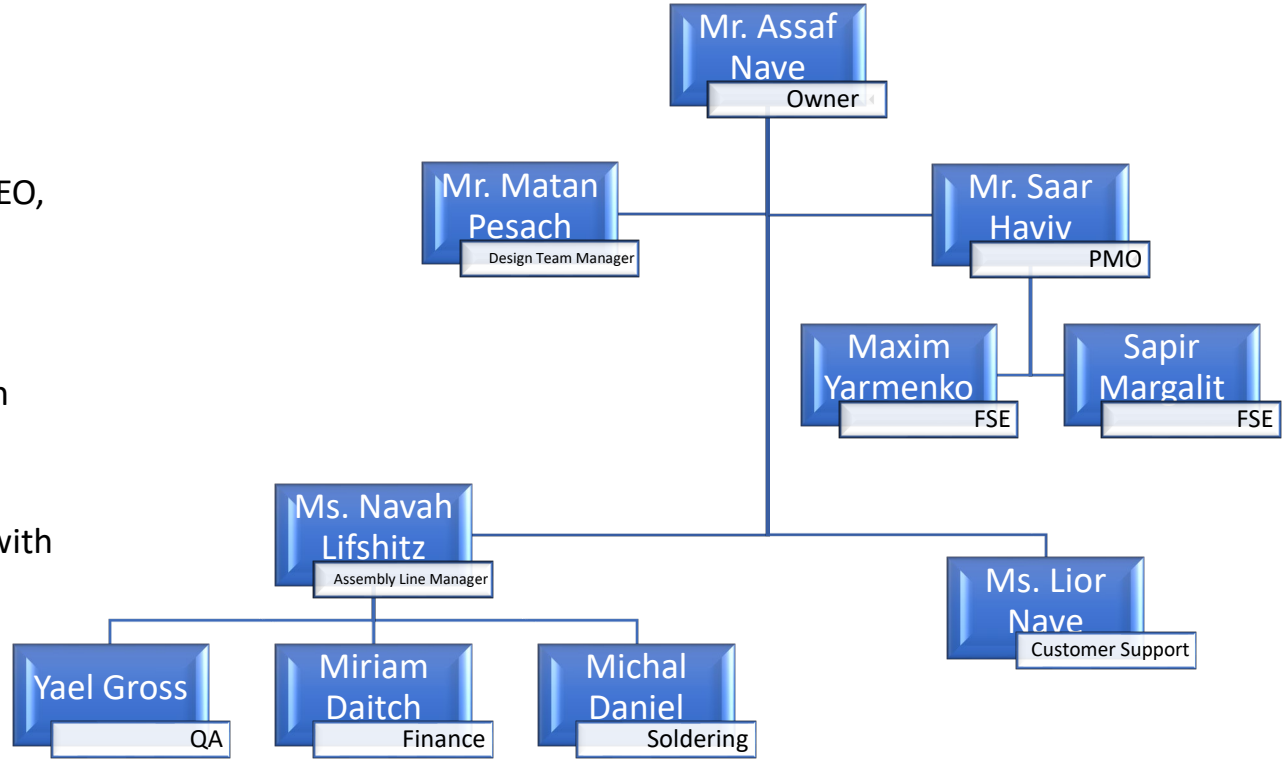
Each department is led by an expert who reports directly to the CEO, ensuring clear lines of communication.

Efficient Decision-Making

This structure allows efficient decision-making and alignment with company objectives.

Our company is structured into several key departments, staring with Product Development, Fabrication and Assembly , Support.

structure allows for efficient decision-making and clear lines of communication, ensuring that our company's objectives are met effectively.



Yearly Development 2014-2025

Product Line Expansion

In 2014, Partnership with Leeno Industrial Inc.

we expanded our product line and entered new markets, showing significant growth and diversification.

Workforce Doubling

By 2017, we had doubled our workforce and increase our growing operations.

Adaptation to Pandemic

In 2020, Partnership with Caliber Interconnect Solutions ,

The pandemic presented challenges, but we adapted quickly with a remote work model and digital transformation.

Sustainability and Community

As of 2023, Partnership with Hon Precision on Handler

Support we focus on sustainability and community engagement, continuing to innovate and grow responsibly.

SAS

Design & Development

Silicon test engineering
IC package design
PCB design
SI/PI Simulation Analysis

LEENO

IC Test Sockets

Build to Spec IC Test Socket Design
Electrical and Thermal Simulation
Cooling Thermal Solutions.

Caliber Interconnect Solutions®

design for perfection

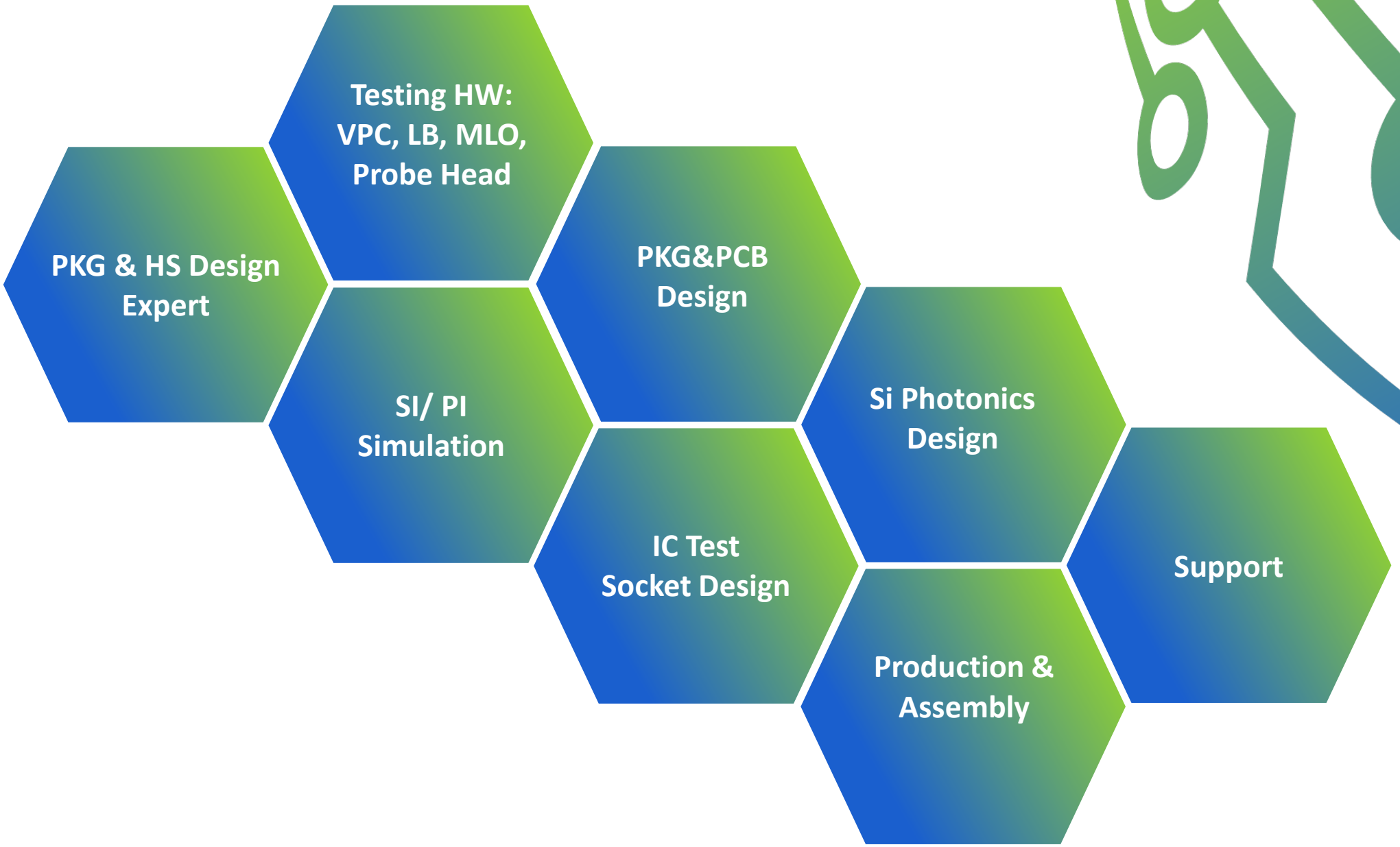
Layout & Simulation

Layout expert in all Cad Tools
Controlling FAB DFM
Gerber and Assy file control

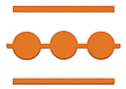
HON.PREC

Handler

HT-1024 / HT-1026 series
HT-1028 / HT-1016 / HT-1032 series
HT-9046MX


Testing HW:
VPC, LB, MLO,
Probe Head
PKG & HS Design
Expert
PKG&PCB
Design
SI/ PI
Simulation
Si Photonics
Design
IC Test
Socket Design
Support
Production &
Assembly

Quantum Device Type

Quantum Device Type	Description	Layout & I/O Needs
 Superconducting Qubits	Josephson junctions, operate on microwave frequencies	GCPW, controlled impedance, cryog enic temperature compattibility
 Quantum Dots	Electrons confined in semiconductor nanostuctures	Dense fanout, low-noise bias lines
 Ion Traps	Trapped ions manipulated with electric fields, laser coling	High voltage control, laser delivery, vacuum compatibility
 Neutral Atoms	Atoms trapped in optical lattices, operated via light	Free-space optics, laser access, magnetic shieldng

Quantum Device Design approach

Quantum System Type	Signal Requirements	Layout Implications	Approach
Superconducting Qubits	Microwave (4–10 GHz), flux bias lines	Impedance-controlled traces, crosstalk isolation	Use CPW or stripline, strict shielding
Quantum Dots	DC bias, fast pulses (GHz)	Dense routing, minimized inductance	Short loops, filtering at chip interface
Ion Traps	RF traps + DC bias	Mixed signal domains, high-voltage zones	RF shield cages, decoupled layers
Spin Qubits	Low-power RF and gate control	Ultra-compact, low-noise	Integrated low-pass filtering, minimal stub vias

QUANTUM HARDWARE R&D SUPPORT

TEST PLATFORMS

•Quantum Device Characterization
Cryogenic test benches for validating qubit prototypes

•Cryogenic Control Chip Evaluation
Boards for testing cryo-compatible DACs, ADCs, and digital-to-qubit signal chains

•Digital Control Chain Testing
Modular setups for pulse pattern control evaluation

•Wafer-Level Test Hardware
Probe cards and automation interfaces for wafer characterization

SAS is Certifiyed By Azenta to Deal with Cryo pico bio storage

QUANTUM HARDWARE R&D SUPPORT

Hardware Area	What SAS Can Deliver
Cryo PCBs & Packaging	Custom boards with cryo-rated materials, HF layout, bonding services
Mixed-Signal Test Chips	Prototype DAC/ADC, PLL, digital drivers
FPGA Pulse Sequencing Boards	Real-time deterministic signal modulation
QPU Interposer Design	Layouts for die-to-board signal transfer, with matched impedances
Evaluation Platforms	Modular test benches, system-level debug environments
Thermal/EMI Fixtures	Design + fabrication of cryo enclosures and heatsinks

Company Medical Certification

CERTIFICATE

This is to certify that the Quality Management System of

Nano-chemika Scientific Solutions Ltd.

24, Ben Josef St., Tel Aviv, Israel

Has been assessed and complies with the requirements of :

ISO 13485:2016

This Certificate is Applicable to

Conformal coating of Parylene. Metal, dielectric and polymeric deposition and coating.

Initial Approval:	15/10/2023		
Valid From:	15/10/2023		
Valid Until:	15/10/2026	**Certificate No.:**	1122144

SII-QCD assumes no liability to any party other than the client, and then only in accordance with the agreed upon Certification Agreement.
This certificate's validity is subject to the organization maintaining their system in accordance with SII-QCD requirements for system certification. The continued validity may be verified via scanning the code with a smartphone, or via website www.sii.org.il. This certificate remains the property of SII-QCD.

Dr. Gilad Golub
CEO

R.N 316140571

Avital Weinberg
Director, Quality & Certification Division

The standards Institution of Israel
42 Chaim Levanon St,
Tel-Aviv 6997701

Page 1 of 1

The Standards Institution of Israel -Your Preferred Choice

BioStore Pico

Service Training Certificate

This is to certify

Saar Haviv

Is now licensed to preform Installation (IQ, OQ PQ), on BioStore Pico system after successfully completing hands on installation and technical training.

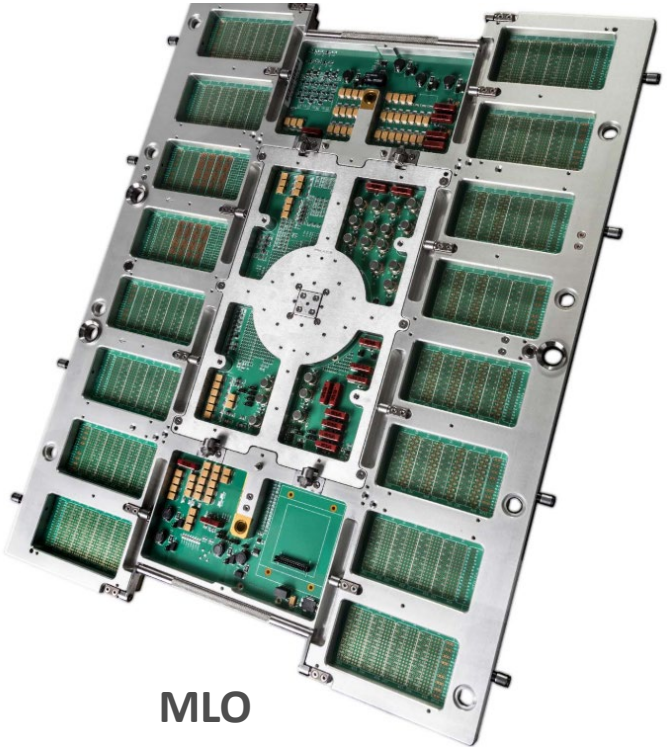
The following topics where covered :

- Operation of the BioStore Pico System
- Installation of the BioStore Pico System
- System Qualification (IQ, OQ PQ)
- Handling of Liquid Nitrogen

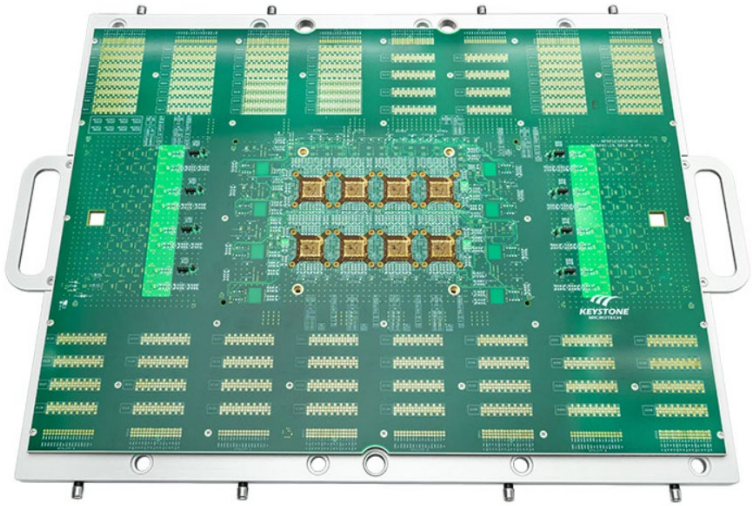
HW Design: VPC, LB, MLO, Probe Head

Advantest	Teradyen	Credence	Chroma
93K EXA	Ultra Flex Plus	D10	Chroma 3360
T2000	UltraFlex	Dx	Chroma 3650
V93K	J750	Fusion MX	
T6575	MicroFlex	Fusion CX	**Others**
T6577	D750	Sapphir	YT5100-S100
EVA100	Catalyst	ASL3000	E320
	Eagle	Quartet	V50
	ETS-88	Schlumberger Fusion	SG9000
	ETS-364		

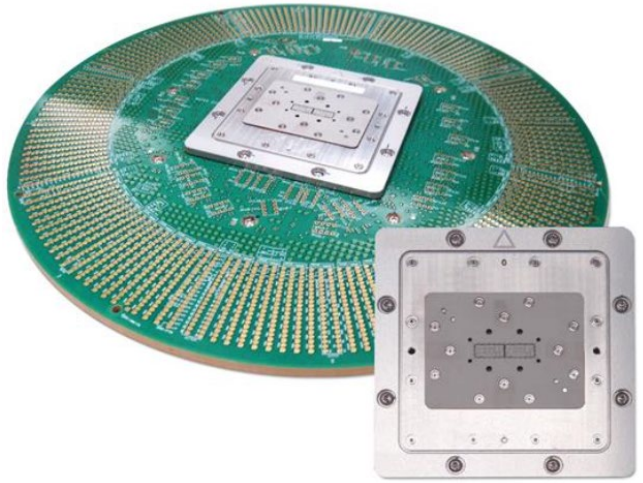
Vertical Probe Card



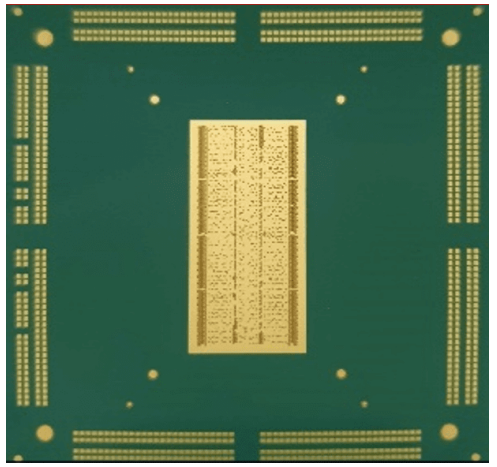
Load Board



Vertical Probe Card



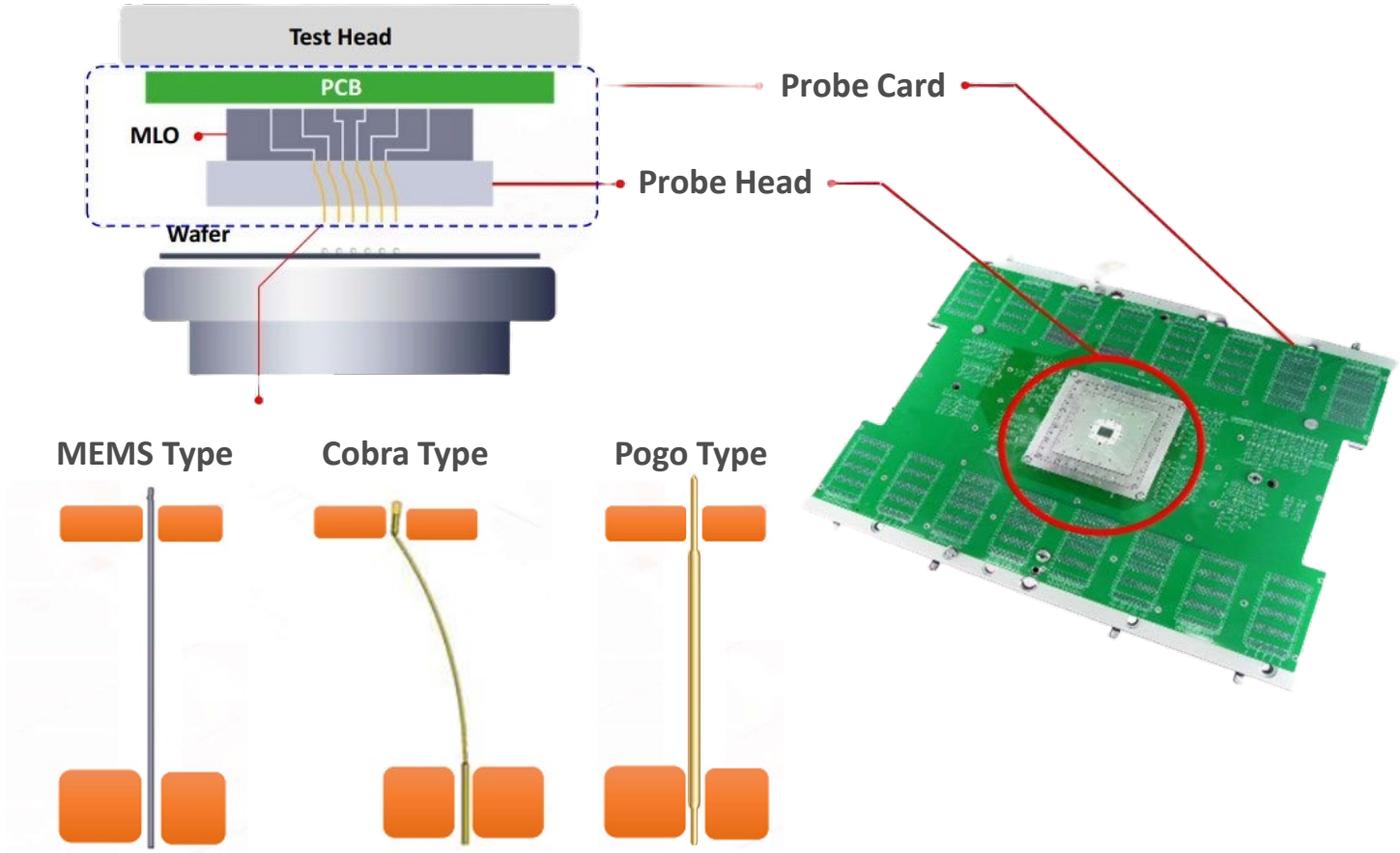
MLO



Testing HW: VPC + MLO + Probe Head Assembly

Probe card is a type of testing device used in semiconductor manufacturing to test integrated circuits (ICs) on a wafer
Probe Head we mainly use 3 type of pins: MEMS, Cobra, Pogo.

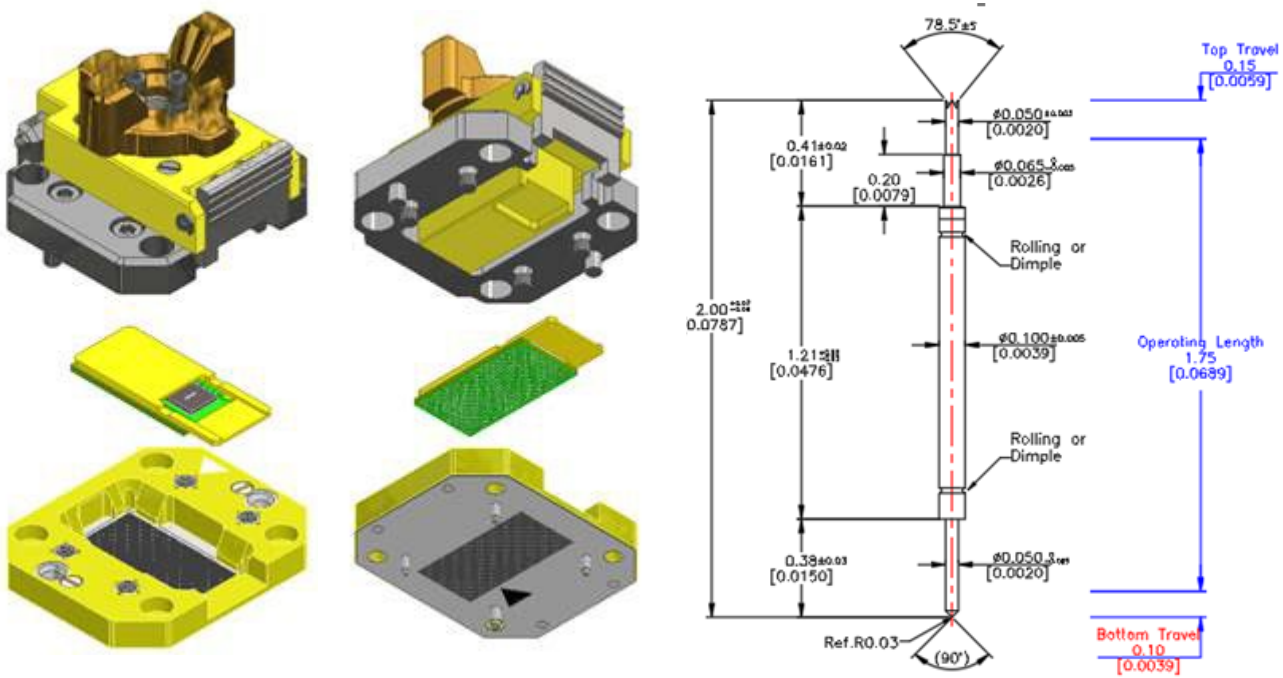
We decide which pin to use per pitch, force, performance and per vendor capability.



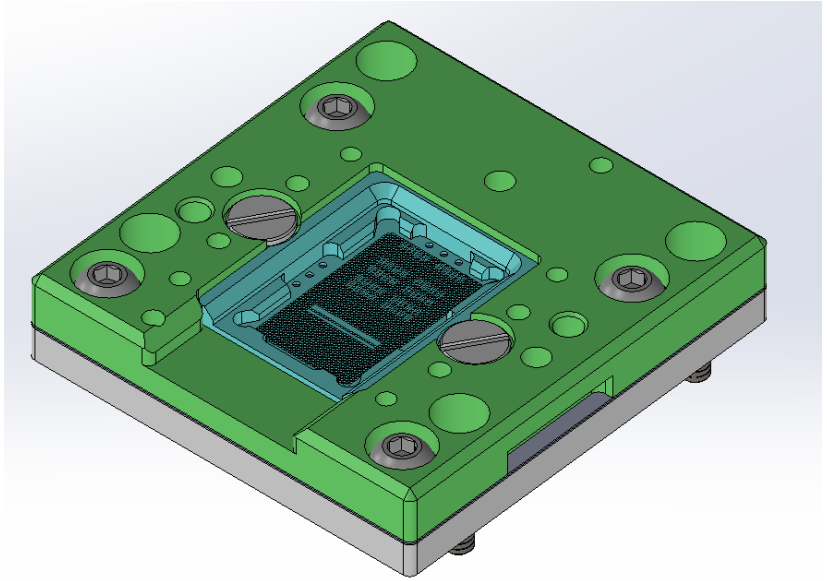
HW Development : Die Level Testing

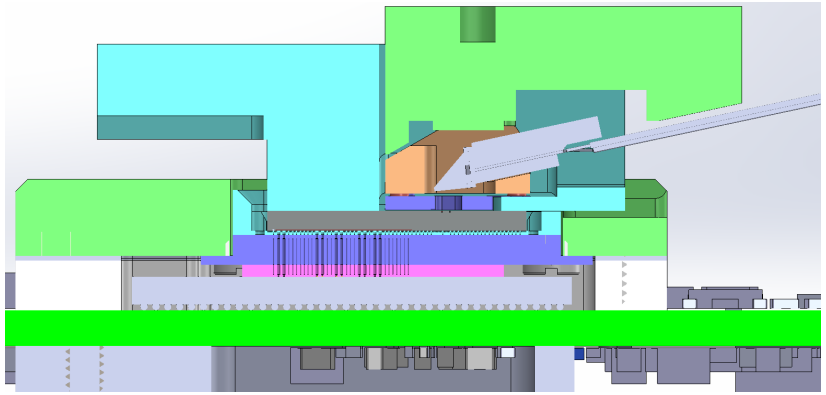
We can support Die Level Testing + Optics.
Minimum pitch is 110um using pogo pin solution.
Maximum frequency is up to 56GHz (40GHz is standard).

Die Level Testing + Cavity for Optics



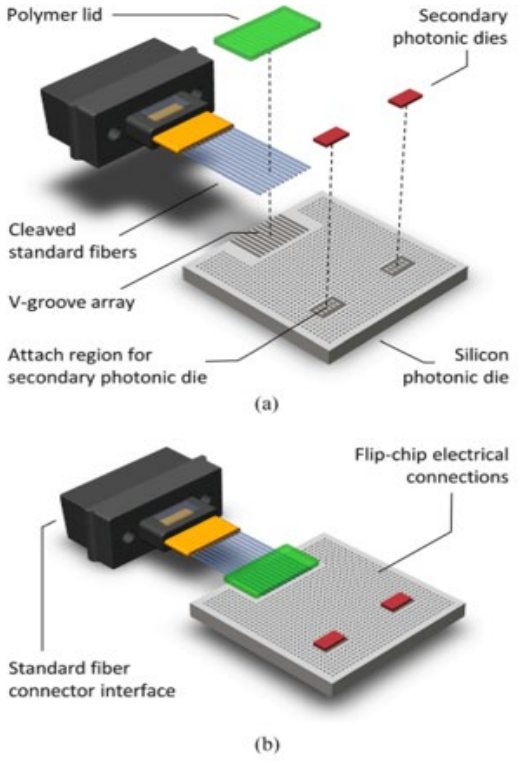
Sagitta X16 – Die Level Testing + Optics

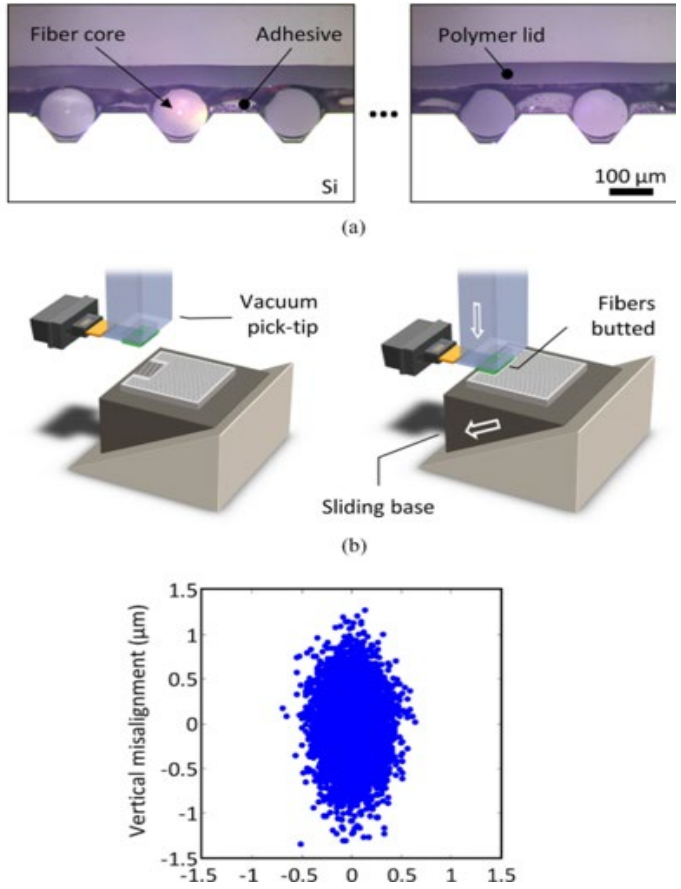


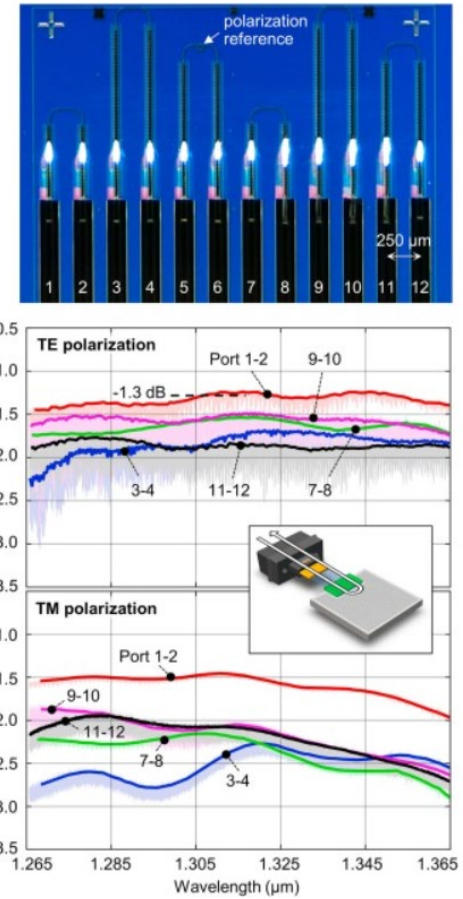


Fiber Coupling V-Groove

Parallelized fiber assembly using V-Grooves features on the Silicon.
V-Groove creates Self Alignment feature thus allowing to meet very strict tolerances of up to +/-2um.
Right now, IBM has experience with 12 Fibers Array coupling and they are working on 16 next.
A peak performance of −1.3 dB is seen on port 1–2 with a 0.7 dB penalty over a ∼100 nm bandwidth and all polarizations.

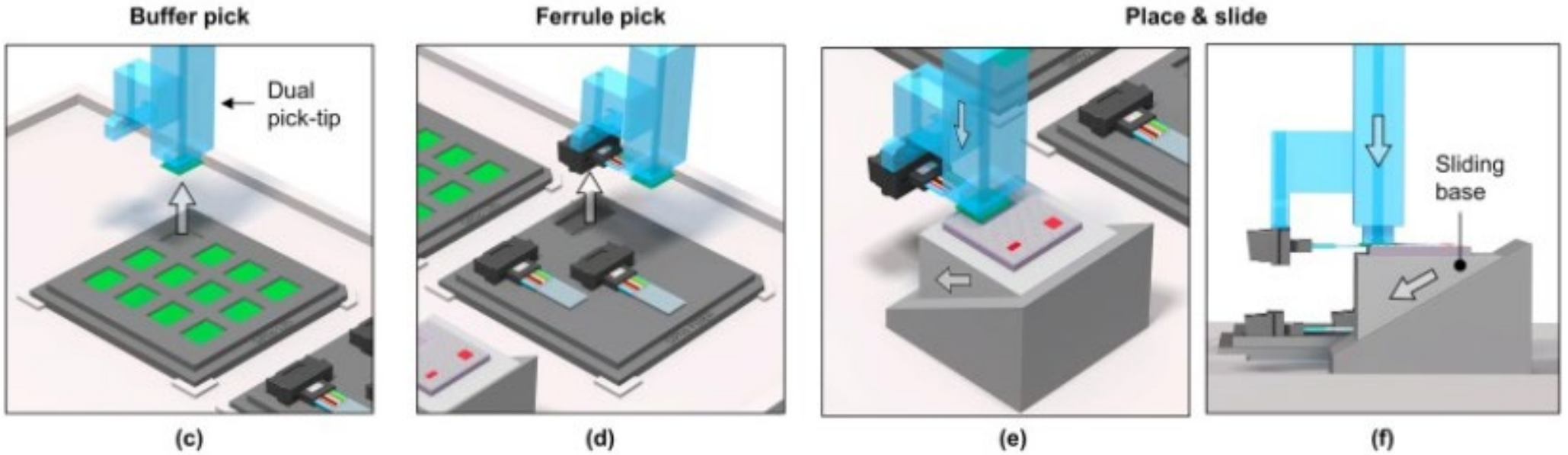


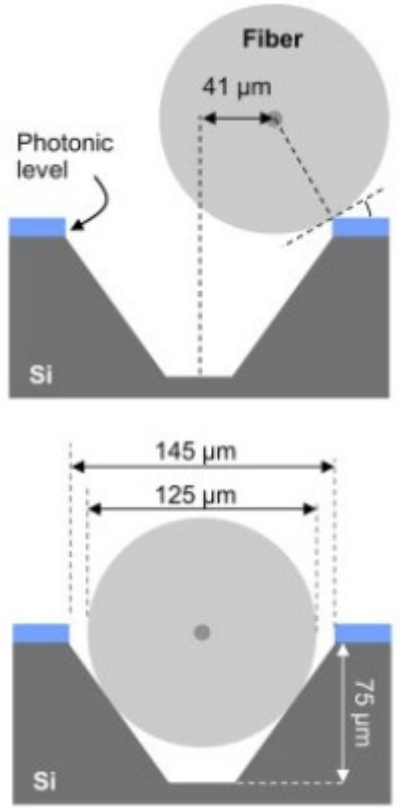




Fiber Coupling V-Groove

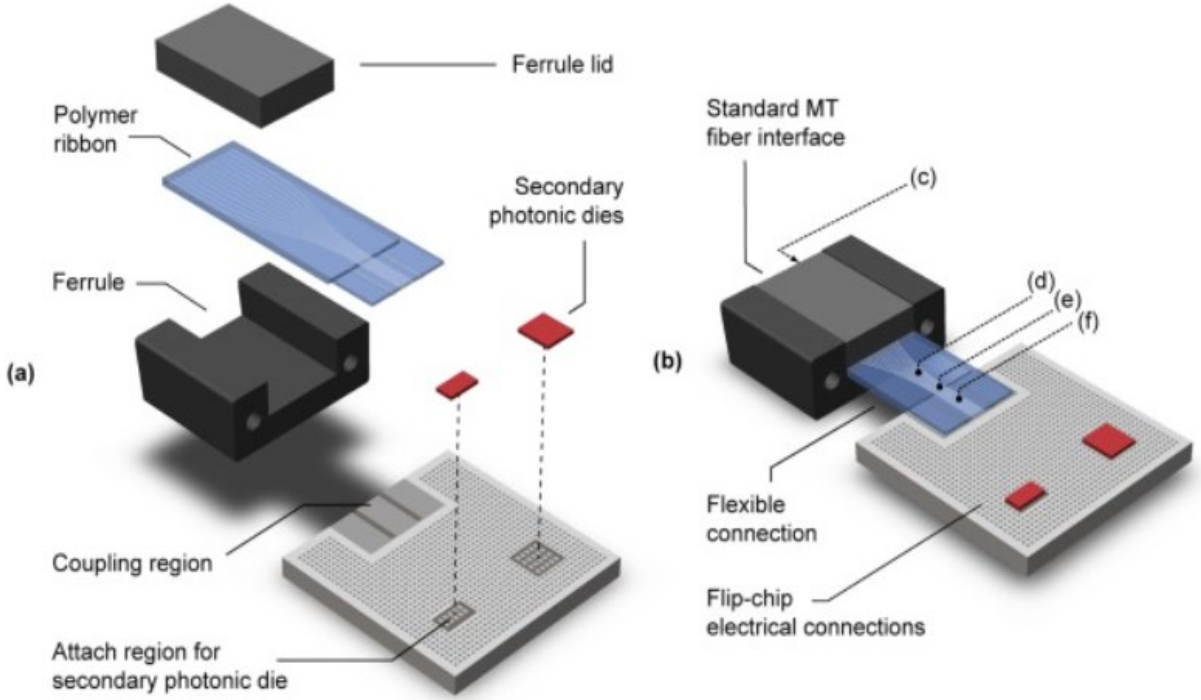
2D & 3D schematics of parallelized fiber assembly.
A polymer buffer is used to prevent tooling contamination with assembly adhesive.
The assembly steps are illustrated in (c)–(f).
A dual vacuum pick-tip, attached to the arm of a standard high-throughput tool,
is used to pick the buffer first and the fiber stub second.
Then, the fiber array is pressed into an integrated V-groove array on chip.
The chip resides on a sliding base that trigonometrically transfers part of the vertical
assembly force into a horizontal force used to butt the fibers on the waveguide couplers integrated on chip.
The sliding base is shown in perspective view in (e) and side view in (f).
Fibers & V-Groove Dimension/Pitch can be seen in the pictures to the right.

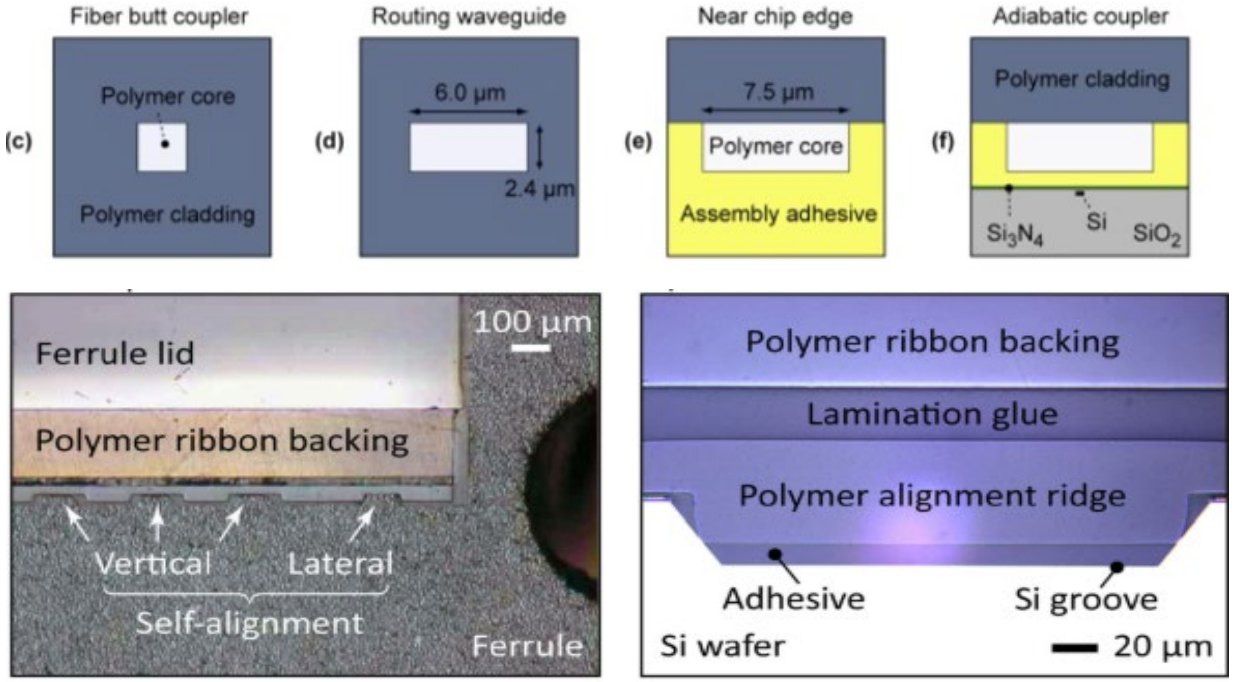




Fiber Coupling Polymer Waveguides

Parallelized fiber assembly using Polymer Waveguides on the Silicon.
lithographically of a Polymer Ribbon and then assembly on ferrule (To support) and fixed by the lid.
This process replicate a standard optical fibers array coupled together to standard MT interface.
The polymer waveguide is then adiabatically widened to a higher-confinement routing waveguide. Any routing design can be used.
The layout used here is a simple pitch transformation from the standard
250µm fiber pitch at the MT interface to a 50µm pitch at the chip interface.
This compliance is expected to improve thermo-mechanical reliability when compared to direct fiber assembly and other rigid connections.
This coupling method results in low package profile and the geometric compatibility with flip-chip electrical connections can notably improve thermal management.
A peak performance of −1.4 dB is seen on port 9–10 with a 0.8 dB penalty over a ~ 100 nm bandwidth and all polarizations



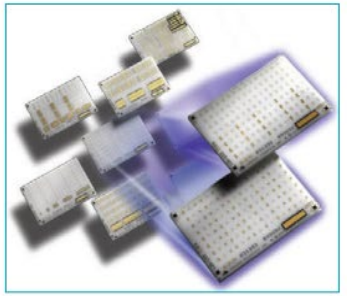


Silicon Photonics – Wafer Level Testing & Calibration

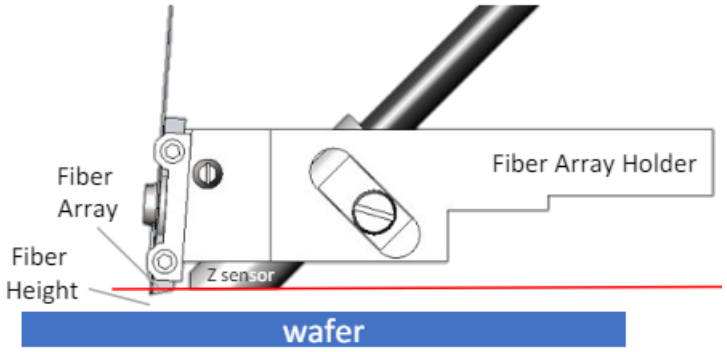
FFI SiPh Wafer-Level Measurement Solution


Single/Dual RF Probes

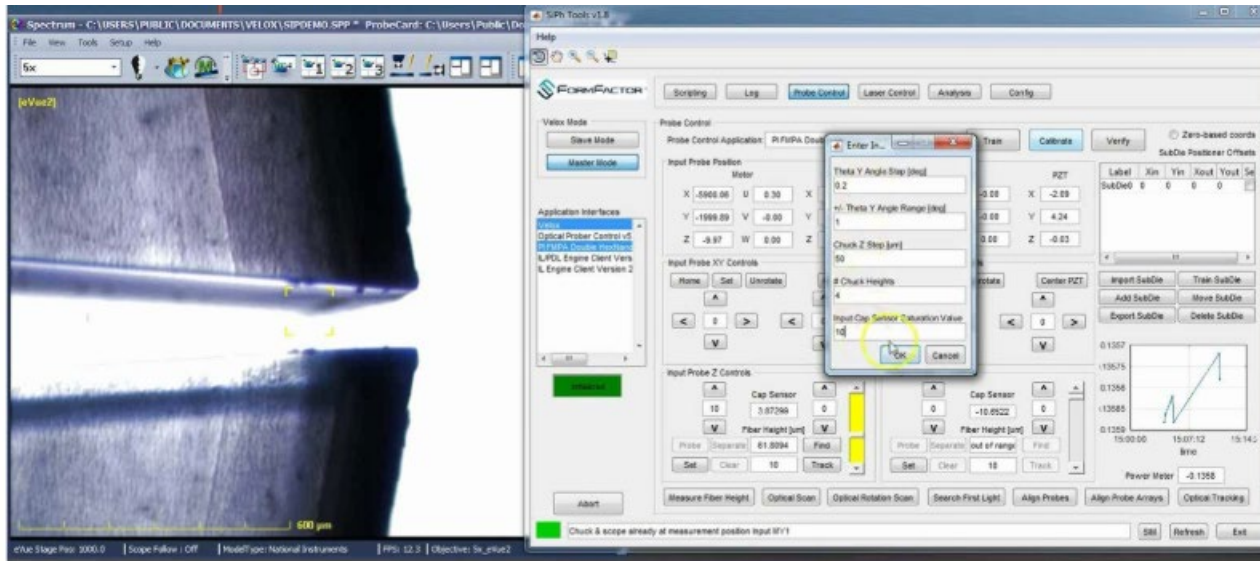

Multi-contact RF Probes


RF Calibration Substrates

RF Calibration Software



Fiber Array @ Y° Incident Angle



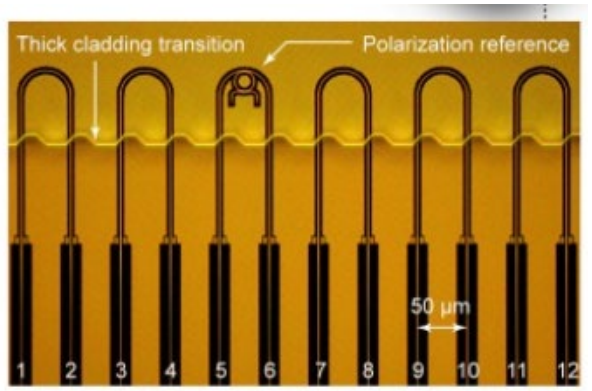
Optical Loopback – Fiber Coupling to PIC

There are three basic approaches

Building a normal (non-photonic) chip, the fabrication is the bulk of the cost and assembly and test is perhaps 20%, while for silicon photonics it is the other way around. Building the chip is cheap, but the cost of the package and the additional steps required for assembly and test make up about 80% of the cost.

- **Active and Powered up**:
  The chip is powered up (in a test mode), the fiber is aligned with the chip, and the chip gives feedback as to how perfect the optical connection is so that the connection can be adjusted
- **Active but not powered up:**
  The fiber is aligned with the chip but it is not powered up. But there are waveguides on the chip that allow the quality of the alignment to be measured externally even so since waveguides transmit light even if not powered up
- **Passive:**
  The assembly process assembles the fiber and the chip in a way that does not depend on feedback about how much light is getting through. Simpler and Cheaper approach for HVM.

Optical Loopback



Support Capability

To ensure the right support , SAS have the following Partnership and Support –

Solid Validation Required Before Delivery

- Taiwan – Zentest , Located in Hsinchu, vast work experiance in TSMC, KYEC, and other OSATS.
- Korea – TFE, Located in Seoul, specialized in BIB, LB, IOT , vast work experience in Amkor.
- India - ArtSemi , Located in Bangalore.

Backup

Israeli Semiconductor Landscape

SAS Technologies LTD.

Israel is Not a “Promised Land” for Semiconductors

Israel, is covered by two-thirds of the desert and has a population of less than 10 million.

In such a small country with harsh conditions, it is home to **nearly 200 semiconductor companies**.

Attracting research and development centers of giants like Nvidia, Intel Apple, Samsung, and Qualcomm.

Through its high-tech industry, Israel has become the only developed country in the Middle East.

How did Israel achieve this? **What has its semiconductor industry experienced?**

After being conquered by the Roman Empire, the Jewish people began a wandering journey that lasted for over 2,000 yeas. Finally, in 1948, the State of Israel was established, providing a homeland for the Jewish people.

They returned to their “promised land.

Places to see while visiting us

Jerusalem

Tel –Aviv

Jaffa

Dead sea

Haifa - Bahá’í Gardens

Testing HW: Probe Assembly Structure

Reflow Process

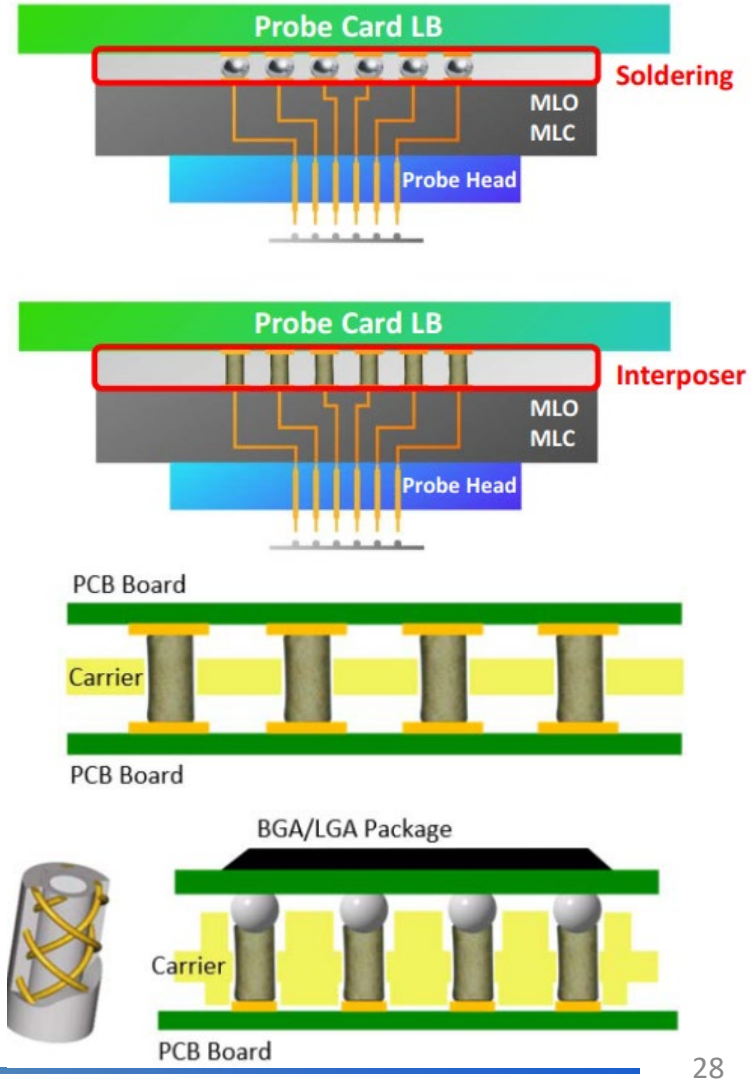
- Consistent temperature environment (vapor chamber)
- Short cycle time
- Lower cost
- Mature & solid process installation

Interposer / i-Bump

- CP (Critical Parameter) compatible with FT (Functional Test)
- Easy to replace space transformer
- Short repair time
- Mechanical strength consideration
- Pitch limited, usually >=0.5mm

i-Bump is made of braided copper-alloy(6/12) wires surrounded by a conductive or non-conductive polymer jacket, which is suitable for board-to-board application and low insertion test solution.

Pitch	0.5 – 1.27mm	Temperature	- 40 to 150℃
Bandwidth	-1dB@20 – 30GHz	Current Rating	3 – 7A（Pitch dependent）

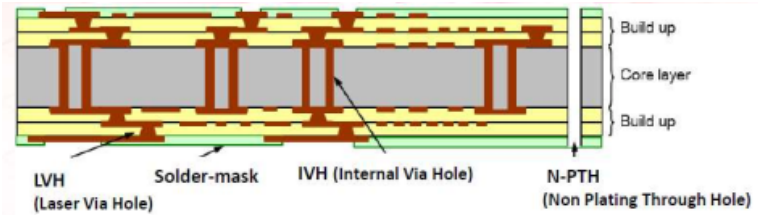


Testing HW: Probe Card High Level DFM

	Pitch >=0.5mm	Pitch=0.35mm	Pitch=0.30mm	Pitch=0.25mm
Board Thickness	8.0→12.0mm	5.58→6.0mm	3.2→4.0mm	3.0→3.5mm
Layer Count (Max)	90L→100L	60L → 68L (Single Lam)	30→40L (Single Lam)	30L→34L (Single Lam)
Drill Dia (mm)	0.2	0.15	0.1	0.1
Aspect Ratio	40:1→60:1	37:1→40:1	32:1→40:1	32:1→40:1
Max 1oz Layer Count	60L→80L	40L→50L	20L→30L	20L→30L
Pin Count (BGA DUT)	24K→32K	16K→24K	8K→16K	3K→5K
BGA pad size (Top)	0.35mm	0.2→0.22mm	0.17mm	0.14mm
Max PCB Size	482.6 X 609.6 mm – 19X24 inch			

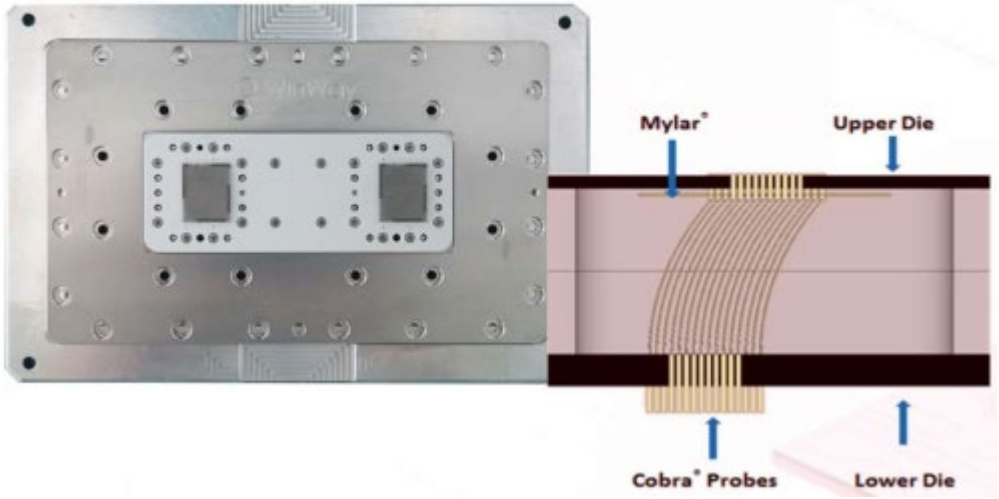
Testing HW: MLO High Level DFM

	Typical Values
Substrate Size (Max)	100X100mm +/-0.2mm
Thickness Range	0.61mm ~ 3.0mm
DUT Bump Pitch (Min)	55um<=
DUT Pad Size (Min)	40um
Laser Via / Pad Size	25um/40um (Top 6 layers) 60um/100um (Below 10L) 40um/60um (Below 10L)
Layer Count (Max)	16-X-16
Impedance Control	+/-10%
Main BU Material	**MCL**: E-705G **MITSUBISHI**: GHPL-972, GHPL-830
Main Core Material	**ABF**: GX-13, GX-92, GL102, GX-T31 **MITSUBISHI**: HL-972, HL-832
Surface Finish	ENEPIG, ENIG, HARD GOLD, OSP



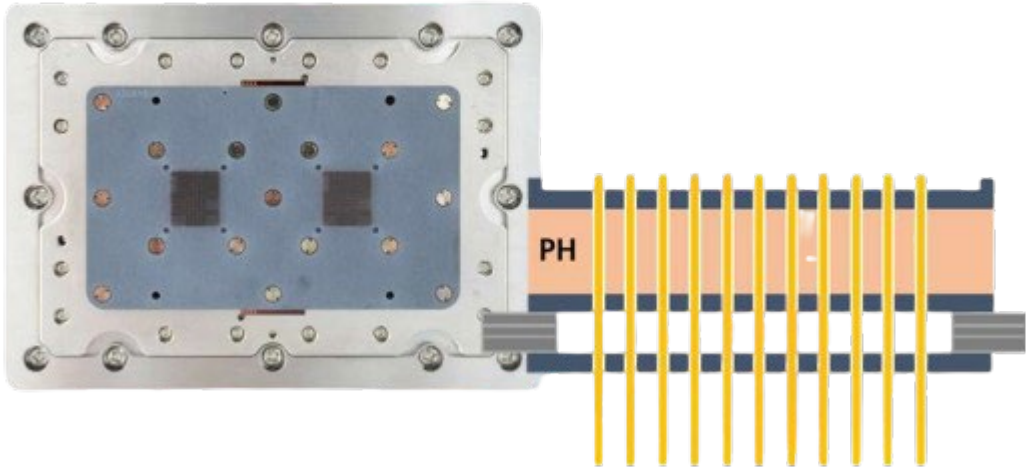
Testing HW: Probe Head Type

Cobra



Max. Pin Count (Experienced)	**Multi-DUT** 30,000 / **Single DUT** 27,000
Lower die material	Machinable Ceramics
Advantage	– High Contact Life & Stability – High Current – Allows stronger contact – Mature Technology

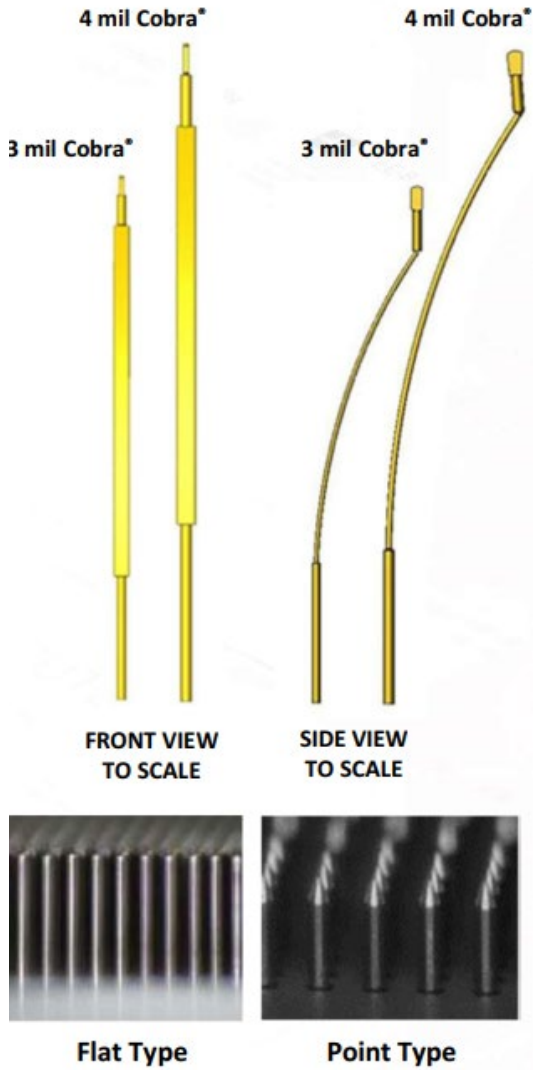
MEMS



Max. Pin Count (Experienced)	**Multi-DUT** 35,000 /**Single DUT** 32,000
Lower die material	Silicon Nitride
Advantage	– High Precision – Miniaturized & High-Density Design – High Parallel Testing Capacity – Lower Contact force

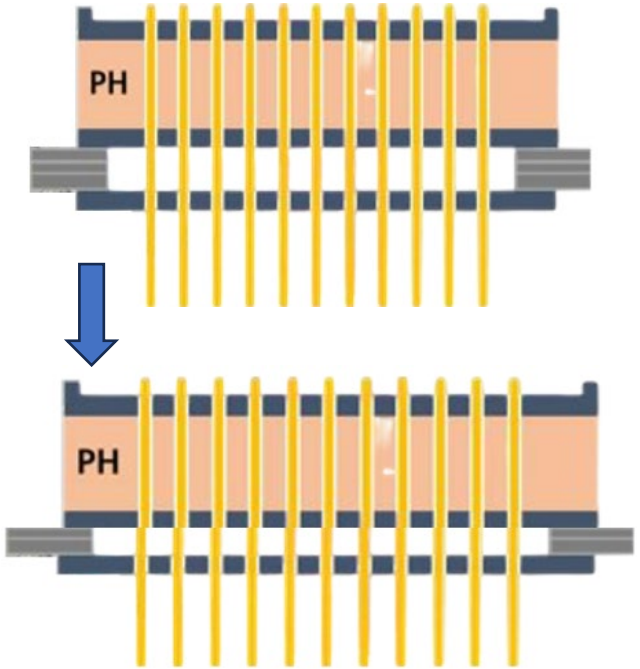
Testing HW: Cobra Pin

Tip Shape	Flat & Point type
Pitch	80 – 200um
Probe diameter	1.8 – 4mils
Tip Length	12 – 36 mils
Min. Pad Size	45um
High C.C.C.	450mA – 2.2A
Temperature	- 50℃ to 150℃
Contact Force	2 – 25gf
Experienced Life Time	3mil → 1.0~1.2 million



Testing HW: MEMS Pin

	WT Series	WS Series
Tip Shape	Flat type	
Pitch	70 – 105um	90 – 130um
C.C.C.	760mA – 1.2A	1.1A – 2.2A
Temperature	- 45℃ to 175℃	
Contact Force	1.8 – 4.5gf	2.5 – 3.5gf
Experienced Life Time	Regular ≥ 1 Million , ELT Type 2~3 Million	



- To further increase lifetime, ELT option is available by removing shims as probe tips wear.
- The idea of this concept is to restore the tip length a few times during the life span.

Testing HW: Probe Card Testing Capability

PRVX VI Probe Card Analyzer

PB6500 Probe Card Analyzer

Probe Scan Analyzer

Probe Card OQC SPEC

項目Item	檢 查 項 目Check Item	規範值/條件 Specification/Condition
A	Contact Resistance	≦10 Ω
B	Leakage	Group Pin ≦ 3730 nA / IO Pin ≦ 10 nA
C	Planarity	≦1 mil
D	Alignment	≦ 1 mil

Highwire Safty Certufication

CERTIFICATE OF COMPLETION

2024 HIGHWIRE ASSESSED

This acknowledgement certifies that on 03/05/2024

S.A.S Advanced Technologies

has successfully completed the Highwire Independent Safety Assessment Program for the trade

Equipment Supplier (Install and/or Maintenance)

Garrett Burke, *President, Highwire*

HIGHWIRE

Safety Assessment Results

Total Score	**88 / 100**
Injury & Illness	40 / 40 points
No of Fatalities	0:5 points awarded
Days Away	35 / 35
Program Elements	25 / 25 points
Management Systems	23 / 35 points
Review of Safety Manual	Zero discrepancies found

Safety Account Expires: Feb 14, 2025 Injury/Illness Data Valid Until Feb 1, 2025

#2b406fb0-b3b9-429d-a3e5-f3320fe7028c